What is claimed:

1. A method for manufacturing a semiconductor device, the method comprising the steps of:

(a) forming a gate dielectric layer;

(b) forming a first conduction layer on the gate dielectric layer;

(c) forming a first upper layer comprising a material different from the first conduction layer on the first conduction layer;

(d) forming a second upper layer comprising a material different from the first upper layer on the first upper layer

(e) forming sidewall spacers on side walls of the first conduction layer, the first upper layer and the second upper layer;

(f) forming an insulation layer that covers the second upper layer and the sidewall spacers;

(g) planarizing the insulation layer until an upper surface of the second upper layer is exposed;

(h) removing the second upper layer;

(i) removing the first upper layer to form a recessed section between the sidewall spacers; and

(j) forming a second conduction layer in the recessed section to form a gate electrode that includes at least the first conduction layer and the second conduction layer.

2. A method for manufacturing a semiconductor device according to claim 1, wherein the step (h) is conducted by an etching method, and in the step (h), a ratio of an etching rate of the second upper layer with respect to an etching rate of the first upper layer is two or greater.

3. A method for manufacturing a semiconductor device according to claim 1, wherein the step (i) is conducted by an etching method, and in the step (i), a ratio of an etching rate of the first upper layer with respect to an etching rate of the first conduction layer is two or greater.

4. A method for manufacturing a semiconductor device according to claim 1, wherein the first upper layer is formed from silicon nitride and the second upper layer is formed from polysilicon.

5. A method for manufacturing a semiconductor device according to claim 1, further comprising, after step (i), forming a barrier layer between the first conduction layer and the second conduction layer.

6. A method for manufacturing a semiconductor device according to claim 1, further comprising, after step (i), forming a barrier layer between the first conduction layer and the second conduction layer, and forming the barrier layer between the second conduction layer and the sidewall spacers.

7. A method for manufacturing a semiconductor device, the method comprising the steps of:

(a) forming a gate dielectric layer;

(b) forming a first conduction layer on the gate dielectric layer;

(c) forming an upper layer on the first conduction layer, at least a lower portion of the upper layer comprising a material different from at least an upper portion of the first conduction layer;

(d) forming sidewall spacers on side walls of the first conduction layer and the upper layer;

(e) forming an insulation layer that covers the upper layer and the sidewall spacers;

(f) planarizing the insulation layer until an upper surface of the upper layer is exposed;

(g) removing the upper layer to form a recessed section between the sidewall spacers on an upper portion of the first conduction layer; and

(h) forming a second conduction layer in the recessed section to form a gate electrode that includes at least the first conduction layer and the second conduction layer.

8. A method for manufacturing a semiconductor device according to claim 7, wherein the step (g) is conducted by an etching method, and in the step (g), a ratio of an etching rate of at least the lower portion of the upper layer with respect to an etching rate of the at least upper portion of the first conduction layer is two or greater.

9. A method for manufacturing a semiconductor device according to claim 7, wherein the first conduction layer is formed from a polysilicon layer.

10. A method for manufacturing a semiconductor device according to claim 7, wherein the second conduction layer comprises a material selected from the group consisting of a metal, a metal alloy and a metal compound.

11. A method for manufacturing a semiconductor device according to claim 7, further comprising, after step (g), forming a barrier layer between the first conduction layer and the second conduction layer.

12. A method for manufacturing a semiconductor device according to claim 7, further comprising, after step (g), forming a barrier layer between the first conduction layer and the second conduction layer, and forming the barrier layer between the second conduction layer and the sidewall spacers.

13. A method for manufacturing a semiconductor device, the method comprising:

forming a gate dielectric layer;

forming a first conduction layer on the gate dielectric layer;

forming an upper layer on the first conduction layer, the upper layer comprising a material different from that of the first conduction layer;

forming sidewall spacers on side walls of the first conduction layer and the upper layer;

removing the upper layer to form a recessed section between the sidewall spacers and above at least part of the first conduction layer; and

forming a second conduction layer in the recessed section to form a gate electrode comprising the at least part of the first conduction layer and the second conduction layer.

14. A method for manufacturing a semiconductor device according to claim 13, further comprising, after step (g), forming a barrier layer between the first conduction layer and the second conduction layer.

15. A method for manufacturing a semiconductor device according to claim 13, further comprising, after step (g), forming a barrier layer between the first conduction layer and the second conduction layer, and forming the barrier layer between the second conduction layer and the sidewall spacers.

16. A method for manufacturing a semiconductor device according to claim 13, wherein the first conduction layer and second conduction layer comprises materials having different compositions.

17. A method for manufacturing a semiconductor device according to claim 13, wherein the first conduction layer comprises polysilicon and the second conduction layer comprises a material selected from the group consisting of a metal, a metal alloy and a metal compound.

18. A semiconductor device comprising:

a field effect transistor, the field effect transistor including a gate dielectric layer, a gate electrode, sidewall spacer regions, a source region, and a drain region, wherein

the gate electrode includes a first conduction layer and a second conduction layer,

the first conduction layer is formed on the gate dielectric layer,

the second conduction layer is formed above the first conduction layer,

the sidewall spacer regions are formed on side walls of the gate electrode,

an insulation layer is provided adjacent to the sidewall spacer regions, and

a barrier layer is provided between the first conduction layer and the second conduction layer and between the second conduction layer and the sidewall spacer.

19. A semiconductor device comprising:

a field effect transistor, the field effect transistor including a gate dielectric layer, a gate electrode, sidewall spacers, a source region, and a drain region, wherein

the gate electrode includes a first conduction layer and a second conduction layer,

the first conduction layer is formed on the gate dielectric layer,

the second conduction layer is formed above the first conduction layer,

the sidewall spacers are formed adjacent to side walls of the gate electrode, and

an insulation layer is provided adjacent to the sidewall spacers, wherein an upper surface of the insulation layer and an upper surface of the second conduction layer are substantially at the same level.

20. A method for manufacturing a semiconductor device according to claim 18, wherein the first conduction layer is formed from a polysilicon layer.

21. A method for manufacturing a semiconductor device according to claim 18, wherein the second conduction layer comprises at least one material selected from the group consisting of a metal, a metal alloy and a metal compound.